

CLAIMS

What is claimed is:

- 1 1. A computerized method comprising:
2 identifying a first stream of data stored in first source register and a
3 second stream of data stored in a second source register; and
4 performing a bit-level interleaving of the first stream of data and the
5 second stream of data to generate a combined stream of data.

- 1 2. The method of claim 1 wherein performing bit-level interleaving
2 further comprises:
3 receiving an interleaving instruction; and
4 executing the interleaving instruction on the first stream of data and
5 the second stream of data.

- 1 3. The method of claim 1 wherein the combined stream of data is stored
2 in a destination register.

- 1 4. The method of claim 3 wherein executing the interleaving instruction
2 further comprises:
3 moving each data bit of the first stream to a corresponding even
4 position of the destination register; and
5 moving each data bit of the second stream to a corresponding odd
6 position of the destination register.

1 5. The method of claim 1 wherein each of the first stream and the second
2 stream includes 16 bits of encoded data.

1 6. An apparatus comprising:
2 an instruction memory to store an interleaving instruction;
3 an instruction sequencer, coupled to the instruction memory, to receive
4 the interleaving instruction;
5 an execution unit, coupled to the instruction sequencer, to execute the
6 interleaving instruction, the interleaving instruction facilitating a bit-level
7 interleaving of a first stream of data and a second stream of data into a
8 combined stream of data; and
9 a register file, coupled to the execution unit, the register file including a
10 first source register to hold the first stream of data, a second source register to
11 hold the second stream of data, and a destination register to hold the
12 combined stream of data.

1 7. The apparatus of claim 6 wherein the execution unit is to execute the
2 interleaving instruction by moving data bits of the first stream to even
3 positions of the destination register and moving data bits of the second stream
4 to odd positions of the destination register.

1 8. The apparatus of claim 6 wherein each of the first stream and the
2 second stream includes 16 bits of encoded data.

1 9. A computer system comprising:
2 a memory to store computer data and instructions; and
3 a processor, coupled to the memory, to receive a first stream of data, a
4 second stream of data, and an interleaving instruction from the memory, to
5 store the first stream of data in a first source register and a second stream of
6 data in a second source register, and to execute the interleaving instruction on
7 the first stream of data and the second stream of data, the interleaving
8 instruction facilitating a bit-level interleaving of the first stream of data and
9 the second stream of data into a combined stream of data.

1 10. The system of claim 9 wherein the processor comprises a destination
2 register to hold the combined stream of data.

1 11. The system of claim 10 wherein the processor is to execute the
2 interleaving instruction by moving data bits of the first stream to even
3 positions of the destination register and moving data bits of the second stream
4 to odd positions of the destination register.

1 12. The system of claim 9 wherein each of the first stream and the second
2 stream includes 16 bits of encoded data.

1 13. A computer readable medium that provides instructions, which when
2 executed on a processor, cause said processor to perform operations
3 comprising:

4 identifying a first stream of data stored in a first source register and a
5 second stream of data stored in a second source register; and
6 performing bit-level interleaving of the first stream of data and the
7 second stream of data to generate a combined stream of data.

1 14. The computer readable medium of claim 13 providing further
2 instructions causing the processor to perform operations comprising:
3 receiving an interleaving instruction; and
4 executing the interleaving instruction on the first stream of data and
5 the second stream of data.

1 15. The computer readable medium of claim 13 wherein the combined
2 stream of data is stored in a destination register.

1 16. The computer readable medium of claim 15 providing further
2 instructions causing the processor to perform operations comprising:
3 moving each data bit of the first stream to a corresponding even
4 position of the destination register; and
5 moving each data bit of the second stream to a corresponding odd
6 position of the destination register.

1 17. The computer readable medium of claim 13 wherein each of the first
2 stream and the second stream includes 16 bits of encoded data.